State of the Art

Greyscale and Time-Uncorrelated Imaging

Since the introduction of solid-state optical sensors, the main trend has been an increase in pixel density at lower costs and higher miniaturisation. Frame rate has been a concern until video rates could be achieved. Until recently, fast cameras have been relegated to niche markets in science and entertainment. However, as soon as higher-than-video speeds have been available, new previously unthinkable applications have emerged [1,2,3,4,5]. Other fields, particularly neuroscience, have also taken advantage of the increased speed to gain dynamic range by trading it off with frame rate [6,7,8]. Many areas of bio-medicine are becoming increasingly dependent on high-speed imaging, due to the importance of chemical dynamics, for example, to understand the interaction between the human genome and its environment. Research is attempting to answer questions on how cells process and exchange information. Understanding intra-cellular chemical waves, for example, may help identify inner-workings of pathogens or the impact of certain pharmaceuticals [9]. Figure 1 shows a high-speed image sequence that enabled the discovery of mechanisms suggesting that chemical waves, not particular proteins to which they may bind, are the target of many pharmaceuticals.

Charge-Coupled Device (CCD) technology is mature [C-2]. In CCDs, photocharges accumulate onto a capacitance. The charge associated with every pixel is then line-wise transferred to the exterior of the pixel array using elaborate mechanisms. The main limitation for a sustained high frame rate in CCDs is the quick and continuous transfer of photo charges across parts or the entire pixel array. Analogue amplification, sample-and-hold (S/H), and analogue-to-digital (A/D) conversion may contribute further to slow CCDs down.

The CMOS Active Pixel Sensor (APS) architecture is also beginning to show signs of maturity, with a general deceleration in performance improvements. In CMOS APS systems, the photocurrent of a diode formed at a p-n junction charges a parasitic capacitance. The resulting voltage is locally and globally amplified, sampled, and A/D converted. Parallel A/D conversion performed at the pixel level [10] provides the fastest architectures. Conventional megapixel cameras based on CMOS APS can reach today speeds of a few thousand frames per second (fps) at full resolution and up to 250,000fps at vastly reduced resolutions and impractical picture aspect ratios [11]. In addition, the dynamic range of single-image cameras is limited to a few tens of dB at normal illumination levels and it is further reduced at very high speeds.

Higher frame rates can be achieved in CMOS APSs, CCDs, and even film cameras when opto-mechanical aids, gated photo-intensifiers, or multiple cameras are used in the optical path [12], but only for a few tens of consecutive frames and at reduced dynamic range. In addition, due to moving parts and fragile components, these cameras are often highly sensitive to mechanical shocks and environmental conditions, thus making them expensive to build and to operate. More recently, solid-state, custom CCD devices have been introduced without opto-mechanical aids to sustain frame rates of 1 million fps, but only for slightly over one hundred consecutive frames [13].

All conventional fast cameras discussed thus far are very high-cost solutions, often topping hundreds of thousand Euros, while high power dissipation is generally a major concern. Sensitivity enhancements have been achieved thanks to new materials enabling much lower photodiode parasitic capacitance, thus improving optical gain. In [14], for example, a CMOS APS was demonstrated for very low illumination levels but at a cost of very large pixels, which are unsuitable for operating regimes of multi-million fps.

At European level, a few R&D projects have dealt or are dealing with imagers, amongst them WALORI (compact low cost camera feasibility demonstration), EDEL (logarithmic response CMOS sensor for automotive applications), HIPSCAN (CMOS image sensor for document acquisition applications), and OMNIVIEWS (space-variant CMOS visual sensors for panoramic imaging). None of them was however focused on time-correlated single photon mode of detection, high native dynamic range, and ultra-high speed imagers implemented in conventional CMOS technologies.Single Photon Counting and Time-Correlated Imaging

Single photon counting operation is not possible with conventional solid-state sensors, thus drastically reducing their impact in pre-eminently single photon applications. In addition, and more importantly, none of these devices can be operated in time-correlated mode with picosecond timing resolution, as required in emerging imaging techniques. In fact, even the fastest reported camera cannot achieve better than 5ns timing resolution, at illumination intensities that destroy most of the delicate bio-materials under test [1].

However, new imaging systems are emerging whereby single photon highly timing-accurate operation is critical. Examples of such need are in fluorescence decay measurements [15], Fluorescence Lifetime Imaging (FLIM) and Fluorescence Correlation Spectroscopy (FCS) [16,17,18], DNA sequencing [14], flow cytometry, etc. As an illustration, Figure 3 shows a setup for single molecule counting based on FCS. Single photon sensitivity can also be beneficial in reducing the complexity of fluorometer systems by replacing laser stimuli by LEDs [19] and by applying frequency domain [20] or space domain signal processing [21].

Researchers have turned increasingly to non-solid-state technologies, such as Photomultiplier Tubes (PMTs). In addition to true single photon sensitivity, PMTs have several advantages in terms of dynamic range, noise, and timing accuracy. A major disadvantage is their cost, size, and the fact that large arrays of PMTs are impractical. More compact multi-channel plate-based, multi-pixel devices have been fabricated [22]. However, these devices still require bulky vacuum chamber apparatuses.

Only recently, single photon counting devices have been successfully integrated in non-deep-submicron CMOS technologies [23]. This achievement has opened the way to non-PMT based fully solid-state single photon imagers. The core of the proposed ultra-fast sensor is a photosensitive device class known collectively as Single Photon Detector (SPD). There exist several implementations of SPDs today, fabricated in non-silicon and non-standard technologies. Due to the need to perform significant processing on chip and an aggressive miniaturisation, we propose to implement SPDs in CMOS using an avalanche diode operated in the socalled Geiger mode. The avalanche process in solid-state devices has been known for at least fifty years, as has its application to photo-multiplication. An avalanche is triggered when reverse biasing a PN-junction to around the breakdown voltage. This effect can be used in two modes of operation. Commonly, the avalanche photodiodes are biased just below the breakdown voltage, the photocurrent remaining proportional to the incoming light intensity. Gain values of a few hundred are obtained in III-V semiconductors as well as in silicon. This mode of operation has been extensively studied in the literature [24,25,26]. Alternatively, to detect very weak light intensities, the photodiode can be biased above the breakdown voltage. The optical gain becomes virtually infinite, however one needs a quenching mechanism to stop the avalanche caused by an impinging photon or a thermal event. The pulse of current generated by an avalanche can be easily converted onto a digital signal, thus making the device operate as an optical Geiger counter. Such device is known as Single Photon Avalanche Diode (SPAD).

To date, only a few researchers have been able to fabricate solid-state SPADs [27,28,29,30]. An important technological obstacle has been to avoid the breakdown at the edge of the p/n junction. In III-V materials as Figure 2. Typical FCS setup comprising a microfluidic tunnel for molecule confinement, a beam-splitter, laser source, and a single photon detector. well as in silicon, specific technologies have been developed for diode fabrication. Edge breakdown has been prevented through use of these ad hoc technological steps – usually unavailable in standard CMOS. For this reason, until recently, silicon SPADs have required costly discrete electronics and/or hybrid solutions [31].

With the recent breakthrough of SPAD integration in a 0.8μm CMOS process [23], performance measures, critical for ultra-high speed and time-correlated applications, have been demonstrated [C-3,C-4]. Consequently, there has been a push to reduce array pitch between detectors in arrays to be comparable to that of CMOS APSs [C-1,C-5]. Pitch reduction has inevitably called for feature size reduction. However, to date, SPADs have not been successfully integrated in deep-submicron CMOS technology.

In addition, until recently image pickup devices have posed no problem to the optical section. In fact, the objective lens was simply chosen with the appropriate focal length to accommodate the desired field of view once the detector diagonal is given, and with a numerical aperture adequate to give the desired 'speed' or 'luminosity' of the image pickup yet maintaining a reasonable depth-of-focus. This situation has changed, however, since the advent of CMOS APS, whereby on-board active circuits occupy a significant fraction of the area next to the active photodetector area, and the resulting fill-factor (the ratio between active and pixel area) is much smaller than 1, resulting in a net loss of sensitivity of the final image detector. As a consequence, one has to compromise between affordable circuit functions and luminous (or radiant) sensitivity of the final photodetector. Single photon counting devices are not immune from this trade-off.

In single photon counting devices the challenge is actually greater due to far smaller fill-factors. To the best of our knowledge, no working example of optical concentrators for use in connection with imaging devices, capable of the concentration and form factors we aim at, has ever been reported in the literature. Optical concentrators have been demonstrated for solar cells [32], but in this case, the aim is just to collect power on a single cell with size of the order of a centimetre. In our case, the dimensions are three orders of magnitude smaller. In addition, massive concentrator arrays must be made with high yields, low cost and be compatible with packaging processes.

At European level, early work on a SPAD 10x1 linear array designed for fabrication by CMOS compatible planar processes was carried out in the MICROSPAD project (1996-99). More recently, a few R&D projects such as EQUIS (completed), RAMBOQ and SECOQC, include research on InGaAs/InP and Si single photon detectors – but not imagers – for quantum communications and quantum processing applications, e.g. for quantum cryptography. In addition, the detectors are usually specifically targeted at the low loss spectral windows for atmospheric transmission (λ~600-850nm) and optical fibre transmission (λ~1.3 and 1.55μm).Literature

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